Amendment to Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously cancelled)

2. (Previously presented) The integrated circuit of claim 8, further comprises a second electrode formed on the ferroelectric layer opposite of the first electrode.

3. (Previously presented) The integrated circuit of claim 8, wherein the spacer comprises of an insulation material.

4. (Previously presented) The integrated circuit of claim 8, wherein the ferroelectric layer comprises of a polymer.

5. (Previously presented) The integrated circuit of claim 8, wherein the support surface comprises of insulation material.

6. (Previously presented) The integrated circuit of claim 8, wherein a portion of the spacer nearest to the first electrode surface has a height about equal to a height of the first electrode, the height of the first electrode being a distance between the support surface and a second electrode surface of the first electrode, the second electrode surface being substantially parallel to the support surface.

7. (Previously presented) The integrated circuit of claim 8, wherein the spacer is in contact with the first electrode surface.

8. (Previously presented) An integrated circuit, comprising:

a first electrode formed on a support surface, the first electrode having a first electrode surface that intersects the support surface;

a spacer positioned on the support surface adjacent to the first electrode surface, wherein the spacer is separated from the first electrode surface; and

a ferroelectric layer formed on the first electrode and the spacer.

9. (Previously presented) The integrated circuit of claim 8, wherein the support surface is located on a die.

10. (Previously cancelled)

11. (Previously presented) The integrated circuit of claim 8, wherein the first electrode comprises first and second portions, the first portion comprising a first material that is non-reactive to the ferroelectric layer and located at a second electrode surface of the first electrode, the second electrode surface being parallel to the support surface, and the second portion comprising a second material that is more conductive than said first material and located between the first portion and the support surface.

12. (Previously cancelled)

13-25 (Cancelled)

26. (Previously presented) The integrated circuit of claim 8, wherein the integrated circuit is a memory circuit.

27. (Previously presented) The integrated circuit of claim 26, wherein the integrated circuit is a non-volatile memory circuit.

28. (Previously presented) The integrated circuit of claim 2, wherein the second electrode adaptedly formed on the ferroelectric layer opposite the first electrode to form a memory cell.

29-31 (Cancelled)

32. (Amended) An integrated circuit, comprising:

a first electrode formed on a support surface, the first electrode having a first electrode surface that intersects the support surface and a second electrode surface that is substantially parallel to the support surface;

a spacer positioned on the support surface adjacent to the first electrode surface, the spacer having a first spacer surface that is substantially in a same plane as the second electrode surface and a second spacer surface that is opposite from the first electrode surface and intersects the support surface~~substantially parallel to the support surface and includes a transition point~~, wherein the spacer is positioned to create a separation distance between the first electrode and a~~the~~ transition point located between the first spacer surface and the second spacer surface ~~, such that the first spacer surface is substantially in a same plane as the second electrode surface~~; and

a ferroelectric layer formed on the first electrode and the spacer, wherein the ferroelectric layer is in contact with at least the first spacer surface and the second spacer surface.

33. (Previously presented) The integrated circuit of claim 32, further comprises a second electrode formed on the ferroelectric layer opposite of the first electrode.

34. (Previously presented) The integrated circuit of claim 32, wherein the spacers are in contact with the first electrode surface.

35. (Currently amended) The integrated circuit of claim 32, wherein the first electrode comprises first and second portions, the first portion comprising a first material that is non-reactive to the ferroelectric layer and located at thea second electrode surface of the first electrode, the second electrode surface being parallel to the support surface, and the second portion comprising a second material that is more conductive than said first material and located between the first portion and the support surface.

36. (Previously presented) The integrated circuit of claim 35, wherein the spacer is formed against the first electrode surface such that the spacer isolates the second portion from the ferroelectric layer.

37. (Previously presented) The integrated circuit of claim 32, wherein the integrated circuit is a memory circuit.

38. (Previously presented) The integrated circuit of claim 37, wherein the integrated circuit is a non-volatile memory circuit.

39. (Previously presented) The integrated circuit of claim 33, wherein the second electrode adaptedly formed on the ferroelectric layer opposite the first electrode to form a memory cell.

40-43 (Cancelled)